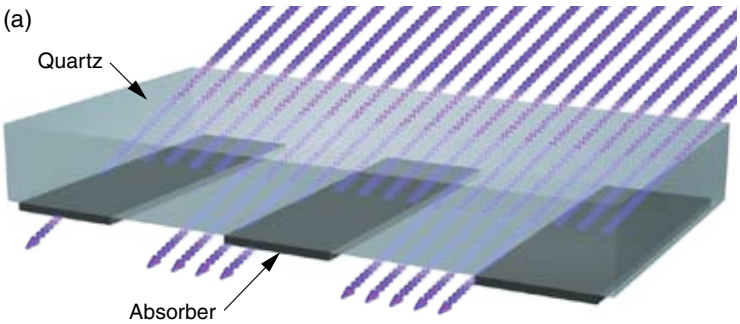
Smoothing Out Defects for Extreme Ultraviolet Lithography

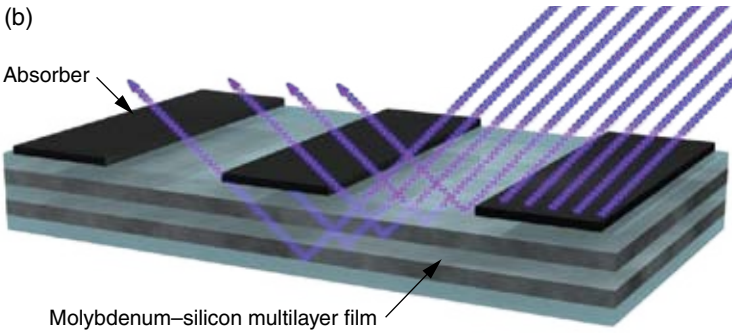
Livermore scientists Paul Mirkarimi (left) and Jeff Robinson examine the mask substrate after it has been smoothed and coated with a molybdenum–silicon reflective multilayer. In the background is the ion-beam deposition and etching system.

SMALLER. Faster. Cheaper. Together, these three words form the mantra of the semiconductor industry as manufacturers search for new methods to increase the computing power of integrated circuits. According to the principle of Moore's Law, the number of transistors on a circuit will double about every two years, and so far, industry has kept up the pace. Photolithography—a process that uses light to "print" a circuit pattern on a semiconductor wafer—has enabled industry to create microchips with nanometer-scale features. Extreme ultraviolet lithography (EUVL) may be the key to continuing Moore's Law into the future, allowing manufacturers to produce even smaller, more powerful microchips.

Current lithographic technologies transmit 193-nanometer-wavelength light through a quartz-based photomask and a series of lenses to create the minute features on microchips. EUVL technology uses light with a much shorter wavelength, 13.5 nanometers. Lenses absorb light at this wavelength rather than transmit it, so EUVL systems include optics to collect and direct light onto a reflective mask. The mask, which contains the pattern for the transistors, reflects the light through another set of optics. These optics reduce the image and direct it onto a silicon wafer coated with photoresist—a light-sensitive material that absorbs the light and retains the projected image. (See *S&TR*, November 1999, pp. 4–9.) The "printed" pattern serves as a guide during the manufacturing process in which portions of the photoresist are chemically removed to create the microchip.

One mask can be used to manufacture tens of thousands of semiconductor wafers, but the pattern on each wafer must be virtually flawless to create a reliable circuit. Tiny imperfections on the mask, such as nanometer-size particles or pits, can transfer defects to the photoresist, causing many chips to fail—a major drawback for an industry that thrives on high-volume production. For EUVL to succeed commercially, the semiconductor industry must reduce these defects to nonprintable sizes. Livermore scientist Paul Mirkarimi, who works in the Chemistry, Materials, Earth, and Life Sciences Directorate, and his colleagues Jeff Robinson and Sherry Baker from the Engineering Directorate along with Eberhard Spiller from the Physical Sciences Directorate have developed such a process. Called ion-beam thin-film planarization,





(a) Masks used in current photolithography systems transmit light through a quartz substrate. (b) In extreme ultraviolet lithography, masks contain a molybdenum–silicon multilayer film that reflects light. In both systems, light exiting the mask travels through a series of lenses that transfer the light onto a semiconductor wafer to create a chip's minute features.

the process planarizes, or smooths, mask defects to create an almost perfectly uniform surface.

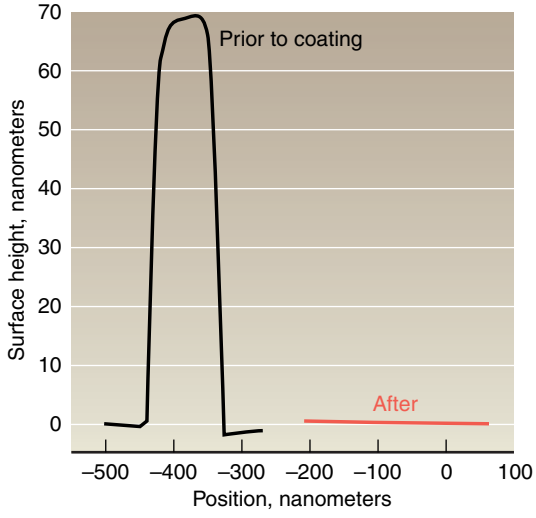
Two Birds with One Stone

An EUVL mask is a substrate coated with a multilayer film of molybdenum and silicon and covered with metal lines that form the pattern for the transistors. Extreme ultraviolet light projected onto the mask is absorbed by the metal and reflected by the multilayer film. The intensity of the reflected light must be uniform to create a usable pattern on the photoresist. Surface perturbations greater than just 1 to 2 nanometers can distort the light enough to create defects in the pattern. The planarization process effectively smooths these defects to less than 1 nanometer.

The smoothing process has two phases. In the first phase, an ion-beam sputtering tool applies a 9-nanometer-thick layer of silicon to the mask substrate. In the second phase, another ion beam etches the silicon, removing about 8 nanometers of the previously deposited layer. These two steps are repeated until the defect is reduced to the required size. Once this smoothing process is complete, multiple layers of molybdenum and silicon are added.

The two-step process earned Mirkarimi and his team an R&D 100 Award in 2003 after the system had successfully planarized substrate particles piled up to 50 nanometers high. (See *S&TR*, October 2003, pp. 10–11.) The researchers have since improved the technique, and it now works effectively on particles up to 80 nanometers.

Over time, manufacturers developed cleaner methods to fabricate masks, significantly reducing the number of substrate particles. Pits, however, were a problem that could not be cleaned away. "Our sponsor, Intel Corporation, encouraged us to work on pits at a time when no one else in the EUVL community was concerned about these defects," says Mirkarimi. "Later, data on mask substrates revealed a significant number of pit defects."



Livermore's ion-beam thin-film planarization process effectively smooths 70-nanometer particles to nonprintable sizes, less than 1 nanometer.

When planarizing particles, the deposition and etching steps are performed at a near-normal angle of incidence. That is, the ion beam is almost perpendicular to the substrate—or approximately 0 degrees to normal incidence. The Livermore researchers found that this method was less effective on pits, at times making the pits larger. However, by adjusting the angle of the substrate during the etching phase, they could eliminate the problem. Placing the ion beam at an off-normal incidence of about 45 degrees produced the required smoothing effects.

Unfortunately, the two approaches were not interchangeable. Each process was effective on only one type of defect: particles or pits. "We then needed to find a method for doing both operations at one time," says Mirkarimi. The team combined the individual processes into a multistep deposition-and-etch system. Deposition still occurs at normal incidence, but etching is performed at two angles, first at off-normal incidence for the pits and then at near-normal incidence for the particles. An etching step follows each deposition step, and defect size determines the total number of deposition-and-etch cycles. In experiments using masks with precise defects, each 70 nanometers in height or depth, the multistep process planarized both particles and pits simultaneously.

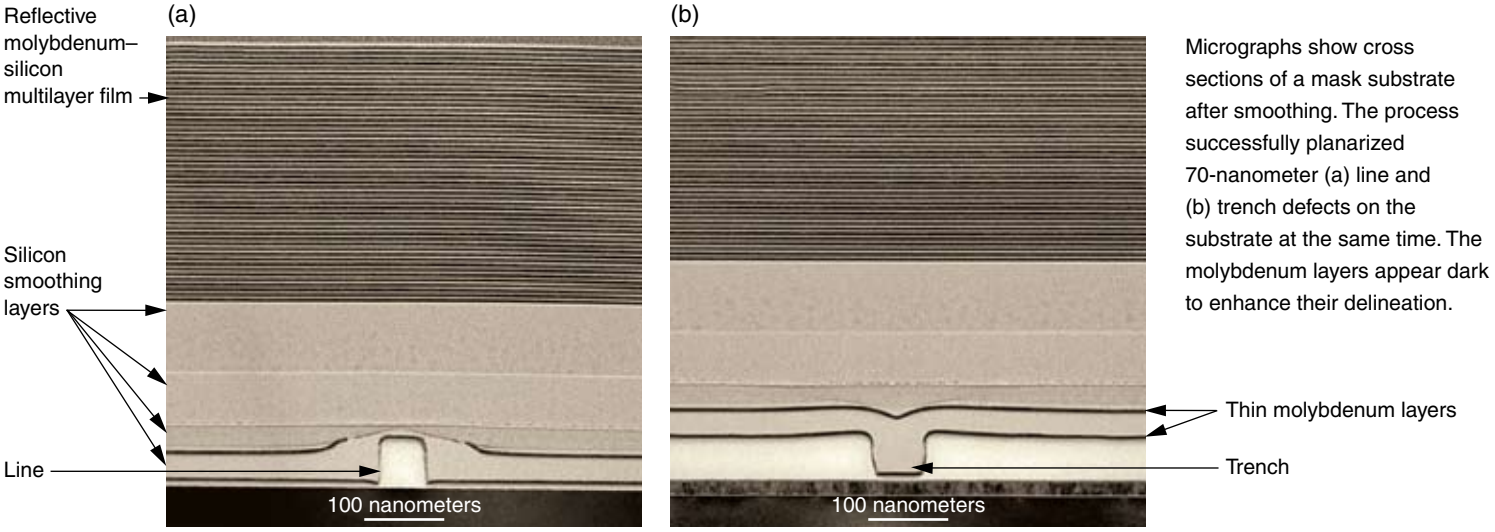
Time Is a Terrible Thing to Waste

In industry, time is money. A smoothing process that takes too long may not be worth the investment to commercialize it. A long processing time is also more likely to introduce additional particles to the mask's surface. When Mirkarimi and his team started their work, the smoothing process took up to 7 hours—too slow for production purposes.

To reduce this time, the team increased the energy of the ion sources by 200 electronvolts for the deposition phase and by 250 electronvolts for etching. These changes increased the deposition rate by 45 percent and the etching rate by 600 percent. The team also adjusted the angles for etching pits from 45 to 52 degrees to compensate for the increased energy from the ion etch source. Together, these modifications reduced the process to about 2 hours.

The team's next challenge was to make the process work on mask defects of varying shapes and sizes. The 70-nanometer particles designed for the Livermore experiments are similar in size to particles found in production environments. Pits, however, can be shallower and wider than the experimental defects. "For this phase of our research, we targeted the largest known pits, which are approximately 18 nanometers deep by 100 nanometers wide," says Mirkarimi. "Once we were successful with the largest pit size, we knew we could smooth the smaller ones."

The team then focused on refining the planarization process to smooth these real-world pits and particles at the same time. Silicon layers are first applied at normal incidence followed by etching at a 70-degree angle for the pits and 0 degrees for the particles.



Micrographs show cross sections of a mask substrate after smoothing. The process successfully planarized 70-nanometer (a) line and (b) trench defects on the substrate at the same time. The molybdenum layers appear dark to enhance their delineation.

This revised method simultaneously planarized the largest pits and particles up to 40 nanometers. The team is confident that the process could be further adjusted to planarize particles with heights up to 50 nanometers.

"We are working on defects that are smaller than anyone has been interested in before," says Mirkarimi. He adds that the semiconductor industry has stringent defect-acceptance specifications. A mask 15 centimeters square can have about 0.0025 defects per square centimeter, which is equivalent to one defect for every two masks. The Livermore planarization process will be needed to produce EUVL masks that meet this specification.

Beyond the 45-nanometer Node

Laboratory researchers have been involved in EUVL research since the mid-1990s. As part of a collaboration known as the Virtual National Laboratory, they worked with colleagues at Lawrence Berkeley and Sandia/California national laboratories to develop EUVL technology. This research was funded through a cooperative research and development agreement with EUV, LLC, a consortium of semiconductor firms, with Intel Corporation as a major contributor.

In 2003, the Virtual National Laboratory began transferring the technology to the semiconductor industry. Intel continued to fund research on the ion-beam thin-film planarization process for another five years in a work-for-others project based out of Livermore's Physical Sciences Directorate. In February 2008, Mirkarimi and his team completed their work, signifying the end of EUVL research at the Laboratory.

Further research and development are needed before the technology will be ready for production. SEMATECH, an organization that helps commercialize semiconductor technology, tested the smoothing process at its Nanotech Center at the University of Albany in New York and obtained results consistent with those achieved at Livermore. Veeco Instruments, Inc., which manufactures mask-coating tools, is helping SEMATECH commercialize the ion-beam thin-film planarization process and has recently developed a multimillion-dollar ion-beam coating and etching tool. This year, Veeco, Inc., and SEMATECH are implementing the faster procedure developed by the Livermore team and making the process cleaner to ensure no new particles are added to the mask during the deposition-and-etch cycles.

The semiconductor industry continues to research other components needed to make EUVL a viable approach for producing computer chips. Livermore's accomplishments have helped move the technology one step closer to production. "If EUVL technology is successful," says Mirkarimi, "it could be the long-term lithography technology the semiconductor industry needs." Because it uses light with an incredibly short wavelength, EUVL has the potential to last for multiple generations of microchips. Manufacturers are currently producing chips with 45-nanometer features, but research is focused on reducing feature size to 32 nanometers and then even smaller. Imagine the technologies that will become available as microchips continue to get smaller, faster, and cheaper.

—Caryn Meissner

Key Words: deposition, etching, extreme ultraviolet lithography (EUVL), integrated circuit, ion-beam thin-film planarization process, mask defect, microchip, reflective multilayer, semiconductor industry, transistor.

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